

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	(formal adj verification) with cutpoint	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/07 15:12
L2	18	netlist with met with timing with constraint	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/07 15:12
S1	809	static adj timing adj analysis	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/03 13:14
S2	2958	timing adj analysis	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/03 13:14
S3	305	(critical adj3 path) and (non-critical adj3 path)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/03 13:15
S4	311	(critical adj3 path) and (non adj critical adj3 path)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/03 13:15
S5	311	S3 or S4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/03 13:15
S6	30	S1 and S5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/03 13:16

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S7	60	S2 and S5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/03 13:16
S8	375	cutpoint	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/03 13:16
S9	2	S7 and S8	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/03 13:17
S10	2	S5 and S8	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/03 13:17
S11	144	final adj3 netlist	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/03 13:17
S12	4325	timing adj3 constraint	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/03 13:18
S13	60	S6 or S7	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/03 13:18
S14	33	S12 and S13	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/03 13:18

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S15	2	S11 and S14	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/03 13:19
S16	2	S8 and S13	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/03 13:20
S17	33	S7 and S12	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/03 13:20
S18	5140	netlist	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/03 13:20
S19	26	S17 and S18	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/03 13:41
S20	622	formal adj verification	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/03 13:42
S21	2	(formal adj verification) with cutpoint	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/03 13:42
S22	4299	(716/4-6).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/03 13:43

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S23	0	(static adj timing adj analysis) and "not check\$3"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/07 15:03
S24	0	(static adj timing adj analysis) and "not adj3 check\$3"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/07 15:03
S25	0	(static adj timing adj analysis) and ("not" adj3 check\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/07 15:03
S26	57	(static adj timing adj analysis) and (formal adj verification)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/07 15:05
S27	375	cutpoint	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/07 15:04
S28	2	S26 and S27	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/07 15:04
S29	841041	critical	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/07 15:05
S30	16516	non-critical or noncritical or (non adj critical)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/07 15:06

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S31	15211	S29 and S30	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/07 15:06
S32	6	S26 and S31	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/07 15:06



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IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

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- ☐ 1. **Static timing analysis for self resetting circuits**
 Narayanan, V.; Chappell, B.A.; Fleischer, B.M.;
[Computer-Aided Design, 1996. ICCAD-96. Digest of Technical Papers., 1996 IEEE/ACM International Conference on](#)
 10-14 Nov. 1996 Page(s):119 - 126
 Digital Object Identifier 10.1109/ICCAD.1996.569415
[AbstractPlus](#) | Full Text: [PDF\(748 KB\)](#) IEEE CNF
[Rights and Permissions](#)
- ☐ 2. **Silicon debug: avoid needles respins**
 de Boer, W.; Vermeulen, B.;
[Electronics Manufacturing Technology Symposium, 2004. IEEE/CPMT/SEMI 29th International Jul 14-16, 2004 Page\(s\):277 - 281](#)
 Digital Object Identifier 10.1109/IEMT.2004.1321676
[AbstractPlus](#) | Full Text: [PDF\(930 KB\)](#) IEEE CNF
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- ☐ 3. **Integrating DFT in the physical synthesis flow**
 Guiller, L.; Neuveux, F.; Duggirala, S.; Chandramouli, R.; Kapur, R.;
[Test Conference, 2002. Proceedings. International](#)
 7-10 Oct. 2002 Page(s):788 - 795
 Digital Object Identifier 10.1109/TEST.2002.1041832
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- ☐ 4. **False timing path identification using ATPG techniques and delay-based information**
 Jing Zeng; Abadir, M.; Abraham, J.;
[Design Automation Conference, 2002. Proceedings. 39th](#)
 10-14 June 2002 Page(s):562 - 565
 Digital Object Identifier 10.1109/DAC.2002.1012688
[AbstractPlus](#) | Full Text: [PDF\(515 KB\)](#) IEEE CNF
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- ☐ 5. **Some conditions under which hierarchical verification is O(N)**
 Scheffer, L.K.;
[Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on](#)
 Volume 22, Issue 5, May 2003 Page(s):643 - 646
 Digital Object Identifier 10.1109/TCAD.2003.810740
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(262 KB\)](#) IEEE JNL
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IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

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1 [An approach to formal verification of real time concurrent Ada programs](#)



Douglas J. Howe, Stephen Michell

 September 2003 **ACM SIGAda Ada Letters , Proceedings of the 12th international workshop on Real-time Ada IRTAW '03**, Volume XXIII Issue 4

Publisher: ACM Press

 Full text available: pdf(287.70 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#)

The SPARK system provides static analysis tools for a highly restricted sequential Ada subset, including a proof checking tool for verifying partial correctness properties. Recently, SPARK Ada has been extended to include much of the Ravenscar Tasking Profile which supports construction of high integrity real time systems. However, the verification machinery has not been changed, and can only handle purely sequential properties of the code. This paper sketches an approach to reasoning about the code.

2 [Computer Communication Networks: Approaches, Objectives, and Performance Considerations](#)



Stephen R. Kimbleton, G. Michael Schneider

 September 1975 **ACM Computing Surveys (CSUR)**, Volume 7 Issue 3

Publisher: ACM Press

 Full text available: pdf(3.99 MB) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

3 [Symbolic algorithms for layout-oriented synthesis of pass transistor logic circuits](#)



F. Ferrandi, A. Macii, E. Macii, M. Poncino, R. Scarsi, F. Somenzi

 November 1998 **Proceedings of the 1998 IEEE/ACM international conference on Computer-aided design**

Publisher: ACM Press

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